## REMARKS

Pursuant to the present amendment, claims 30-31, 35-36 and 40-41 have been amended. Claims 1-9, 22 and 26-41 are pending in the present application. No new matter has been introduced by way of the present amendment. Reconsideration of the present application is respectfully requested in view of the amendments and arguments set forth herein.

As an initial matter, claims 30-31, 35-36 and 40-41 have been amended to be consistent with their respective independent claims, *i.e.*, the independent claims recite a layer of gate electrode material, thus the feature has been amended to recite to a gate electrode feature. Entry of the amendment is respectfully requested as it will further clarify the claims for allowance and/or appeal.

In the Office Action, claims 1-5 and 7-8 were rejected under 35 U.S.C. § 102 as allegedly being anticipated by Ishida (U.S. Patent No. 6,344,396). Claims 1-3 and 7 were rejected under 35 U.S.C. § 102 as allegedly being anticipated by Long (U.S. Patent No. 6,153,534). Claims 6, 22 and 26-41 were rejected under 35 U.S.C. § 103 as allegedly being obvious over Ishida or Long in view of Iyer (U.S. Patent No. 6,121,133). Applicants respectfully traverse the Examiner's rejections.

Applicants hereby re-incorporate by reference the arguments for allowability made in the previous response. It is respectfully submitted that the Examiner's continued rejection of the pending claims based upon Ishida and/or Long reflects a fundamental misreading of both of those references. Independent claim 1 clearly recites the step of, after depositing said first layer and said second layer of material, patterning said second layer of material and first layer to form

said semiconductor device feature in said first layer. The references relied upon the Examiner simply fail to disclose at least this significant limitation of independent claim 1.

On page 3 of the Final Office Action, the Examiner states that Ishida discloses depositing a first layer 12 and the second layer 14 and patterning the second layer 14 and the first layer to form a device feature in the first layer. It is respectfully submitted that this statement is just fundamentally at odds with the express disclosure in Ishida. In Ishida, it is clear that the electrode structure 12 is formed prior to the deposition of the second material layer 14. At no point does Ishida even remotely suggest that this first layer of material, *i.e.*, the layer 12, is patterned in any respect after the formation of the second layer of material 14. This is clear from the sequence of drawings depicted in Ishida. Again, it is respectfully submitted that Ishida does not anticipate claims 1-5 and 7-8 as suggested by the Examiner. Moreover, there is simply no motivation in Ishida to modify the references so as to arrive at Applicants' invention. Ishida is concerned with manipulations of the characteristics of the sidewall spacer 14 to ultimately achieve control on the positioning of the drain region. Ishida is simply not concerned with patterning of the layer 12 as that step has already been performed presumably in accordance with known processing techniques.

Long, the Examiner's other primary reference, also suffers from a similar deficiency. In Long, as with Ishida, the semiconductor device feature has already been formed in the underlying first layer prior to the deposition of the second layer of material identified by the Examiner, *i.e.*, the layer 14 in Ishida and the layer 250 in Long.

Applicants respectfully submit that a plain reading of the references identified by the Examiner leads to the inescapable conclusion that all pending claims are allowable over the prior

art. The Examiner is invited to contact the undersigned attorney at (713) 934-4055 with any questions, comments or suggestions relating to the referenced patent application.

Respectfully submitted,

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